SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

Scheme of examination as per AICTE model Curriculum w.e.f July 2020

Grading System

Course Name –Master of Technology (VLSI)

Semester I / Year : I **Scheme for 2020 Admitted Students onwards**

S. No.	Subject Code	Category	Subject Name	Maximum Marks Allotted					Hours/ Week			Credit	Total Marks
				Theory			Practical						
				End Sem.	Mid Sem	Quiz, Assignment	End Sem	Term Work	L	T	P		
1	MTVD 11	CORE	RTL SIMULATION AND SYNTHESIS WITH PLDs	100	30	30	50	50	3	1	4	6	260
2	MTVD 12	CORE	MICRO CONTROLLER AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS	100	30	30	50	50	3	1	4	6	260
3	MTVD 13	CORE	RESEARCH METHODOLOGY AND IPR	100	30	30	-	-	3	1	-	4	160
4	MTVD 14	PE	ELECTIVE-1	100	30	30	-	-	3	1	-	4	160
5	MTVD 15	PE	ELECTIVE-1I	100	30	30	-	-	3	1	-	4	160
6	MTVD 16	AUDIT	AUDIT - I	-	-	-			2	0	0	0	-
TOTAL				**500**	**150**	**150**	**100**	**100**	**17**	**5**	**8**	**24**	**1000**

L: Lecture **T:Tutorial** **P:Practical**

ELECTIVE -I	ELECTIVE -II	AUDIT COURCE- I
MTVD14(A).DIGITAL SIGNAL AND IMAGE PROCESSING	MTVD15(A). PARALLEL PROCESSING	1.ENGLISH FOR RESEARCH PAPER WRITING
MTVD14(B). PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE	MTVD15(B).SYSTEM DESIGN WITH EMBEDDED LINUX	2.DISASTER MANAGEMENT
MTVD14(C).VLSI SIGNAL PROCESSING	MTVD15(C). VLSI DESIGN	3.SANSKRIT FOR TECHNICAL KNOWLEDGE
		4.VALUE EDUCATION

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

Scheme of examination as per AICTE model Curriculum w.e.f July 2020

Grading System

Course Name –Master of Technology (VLSI)

Semester II / Year : I **Scheme for 2020 Admitted Students onwards**

S. No.	Subject Code	Category	Subject Name	Maximum Marks Allotted					Hours/ Week			Credit	Total Marks
				Theory			Practical						
				End Sem.	Mid Sem	Quiz, Assignment	End Sem	Term Work	L	T	P		
1	MTVD 21	CORE	ANALOG AND DIGITAL CMOS VLSI DESIGN	100	30	30	50	50	4	1	4	6	260
2	MTVD 22	CORE	VLSI DESIGN VERIFICATION AND TESTING	100	30	30	50	50	4	1	4	6	260
4	MTVD 23	PE	ELECTIVE III	100	30	30	-	-	4	1	-	5	160
5	MTVD 24	PE	ELECTIVE IV	100	30	30	-	-	4	1	-	5	160
	MTVD 25	CORE	MINI PROJECT WITH SEMINAR	-	-	-	100	60	-	-	4	2	160
6	MTVD 26	AUDIT	AUDIT - II	-	-	-	-	-	2	-	-	-	-
TOTAL				**400**	**120**	**120**	**200**	**160**	**18**	**4**	**8**	**24**	**1000**

L: Lecture **T:Tutorial** **P:Practical**

ELECTIVE -III	ELECTIVE -IV	AUDIT COURSE - II
MTVD23(A) .MEMORY TECHNOLOGIES	MTVD24(A). COMMUNICATION BUSES AND INTERFACES	1. CONSTITUTION OF INDIA
MTVD23(B).SoC DESIGN	MTVD24(B).VLSI TECHNOLOGY	2. PEDAGOGY STUDIES
MTVD23(C) .LOW POWER VLSI DESIGN	MTVD24(C)PHYSICAL DESIGN AUTOMATION	3. STRESS MANAGEMENT BY YOGA
		4. PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

Scheme of examination as per AICTE model Curriculum w.e.f July 2020

Grading System

Course Name –Master of Technology (VLSI)

Semester III / Year : II Scheme for 2020 Admitted Students onwards

S. No.	Subject Code	Category	Subject Name	Maximum Marks Allotted					Hours/ Week			Credit	Total Marks
				Theory			Practical						
				End Sem.	Mid Sem	Quiz, Assignment	End Sem	Term Work	L	T	P		
	MTVD31	PE	ELECTIVE V	100	30	30	-	-	4	1	-	5	160
	MTVD32	OE	OE	100	30	30	-	-	4	1	-	5	160
1	MTVD DP(1)	DESSERTATION	DESSERTATION (PHASE-I)	-	-	-	400	280	-	-	20	10	680
TOTAL				**200**	**60**	**60**	**400**	**280**	**8**	**2**	**20**	**20**	**1000**

L: Lecture **T:Tutorial** **P:Practical**

ELECTIVE -V	OPEN ELECTIVE (OE)
MTVD31(A).CAD OF DIGITAL SYSTEM	MTVD32(A).BUSINESS ANALYTICS
MTVD31(B).SELECTED TOPICS IN MATHEMATICAL	MTVD32(B).OPERATIONS RESEARCH
MTVD31(C).NANO MATERIAL AND TECHNOLOGY	MTVD32(C) COST MANAGEMENT OF ENGINEERING PROJECTS

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

Scheme of examination as per AICTE model Curriculum w.e.f July 2020

Grading System

Course Name –Master of Technology (VLSI)

Semester IV / Year : II **Scheme for 2020 Admitted Students onwards**

S. No.	Subject Code	Category	Subject Name	Maximum Marks Allotted					Hours/ Week			Credit	Total Marks
				Theory			Practical						
				End Sem.	Mid Sem	Quiz, Assignment	End Sem	Term Work	L	T	P		
1	MTVD DP (II)	DESSERTATION	DESSERTATION (PHASE-II)	-	-	-	500	500	-	-	30	15	1000
TOTAL				**-**	**-**	**-**	**500**	**500**	**-**	**-**	**30**	**15**	**1000**

L: Lecture **T:Tutorial** **P:Practical**

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD 11 RTL SIMULATION AND SYNTHESIS WITH PLDs

Unit1:

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static Timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

Unit 2:

Design entry by Verilog/VHDL/FSM, Verilog AMS.

Unit 3:

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

Unit 4:

Design for performance, Low power VLSI design techniques. Design for testability.

Unit 5:

IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping

Unit 6:

Case studies and Speed issues.

References:

- Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
- Donald D Givone, “Digital principles and Design”, TMH
- Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
- Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
- Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx
- Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD 12 MICRO CONTROLLER AND PROGRAMMABLE DIGITAL SIGNAL

Unit 1: ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation Modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

Unit 2: Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

Unit 3:LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

Unit 4: Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

Unit 5: VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations

Unit 6: Code Composer Studio for application development for digital signal processing,
On chip peripherals, Processor benchmarking

References:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH , 2nd Edition

3. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication

4. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education

5. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley

6. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD 13 REASEARCH METHODOLOGY AND IPR

Unit 1

Foundations of Research: Meaning, Objectives, Motivation, Utility. Characteristics of scientific method – Understanding the language of research – Concept, Construct, Definition, Variable, Research process, Problem Identification & Formulation – Research Question – Investigation Question – Measurement Issues – Hypothesis – Qualities of a good Hypothesis –Null Hypothesis & Alternative Hypothesis. Hypothesis Testing – Logic & Importance

Assignment 1: Identify Research Problem based on Trends

Unit 2

Research Design: Concept and Importance in Research – Features of a good research design – Exploratory Research Design – concept, types and uses, Descriptive Research Designs – concept, types and uses. Experimental Design: Concept of Independent & Dependent variables.

Assignment 2: Identify Research methodology for Research Problem identified

Unit 3

Data Analysis: Data Preparation – Univariate analysis (frequency tables, bar charts, pie charts, percentages), Bivariate analysis – Cross tabulations and Chi-square test including testing hypothesis of association.

Assignment3: Propose a method for Data Analysis on Research problem identified

Unit 4

Importance of Literature Review. Interpretation of Data and Paper Writing – Layout of a Research Paper, Journals in Computer Science, Impact factor of Journals, When and where to publish ? Ethical issues related to publishing, Plagiarism and Self-Plagiarism. Use of Encyclopedias, Research Guides, Handbook etc., Academic Databases for Computer Science Discipline.

Assignment 4: Write paper on Literature Review of your research Problem

Unit 5

Use of tools / techniques for Research: methods to search required information effectively, Reference Management Software like Zotero/Mendeley, Software for paper formatting like Latex/MS Office, Software for detection of Plagiarism. Documentation of Research work, Synopsis, Presentations, Writing Research papers on experimentation results, proposed methods, thesis formats

Assignment 5: Write Synopsis for proposed Research Problem

Reference Books:

1. Business Research Methods – Donald Cooper & Pamela Schindler, TMGH, 9th edition
2. Business Research Methods – Alan Bryman & Emma Bell, Oxford University Press.
3. Research Methodology – C.R.Kothari
4. Select references from the Internet.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD 14(A).DIGITAL SIGNAL AND IMAGE PROCESSING

Unit 1:

Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.

Unit 2:

Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation.

Unit 3:

Fixed point implementation of filters – challenges and techniques.

Unit 4:

Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – JPEG and JPEG 2000.

Unit 5:

Color Image processing – Handling multiple planes, computational challenges.

Unit 6:

VLSI architectures for implementation of Image Processing algorithms, Pipelining.

References:

- J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
- Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition
- S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006
- A. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
- KeshabParhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India

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MTVD14 (B). PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE

Unit 1:

Embedded 'C' Programming

- Bitwise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, Code optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

Unit 2:

Object Oriented Programming

- Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

Unit 3:

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

Unit 4:

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

Unit 5:

Templates: Function template and class template, member function templates and template arguments,Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.

Unit 6:

Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

References:

- Michael J. Pont , “Embedded C”, Pearson Education, 2nd Edition, 2008
- Randal L. Schwartz, “Learning Perl”, O’Reilly Publications, 6th Edition 2011
- A. Michael Berman, “Data structures via C++”, Oxford University Press, 2002
- Robert Sedgewick, “Algorithms in C++”, Addison Wesley Publishing Company, 1999
- Abraham Silberschatz, Peter B, Greg Gagne, “Operating System Concepts”, John Willey & Sons, 2005

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MTVD14(C).VLSI SIGNAL PROCESSING

Unit 1:

Introduction to DSP systems, Pipelined and parallel processing.

Unit 2:

Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

Unit 3:

Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise.

Unit 4:

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.

Unit 5:

Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.

Unit 6:

Programmable digit signal processors.

References:

- .Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley, Inter Science, 1999.
- Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
- S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

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MTVD15(A). PARALLEL PROCESSING

Unit 1:

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

Unit 2:

Principles and implementation of Pipelining, Classification of pipelining processors,

Advanced pipelining techniques, Software pipelining

Unit 3:

VLIW processors

Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

Unit 4:

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques,

Principles of multithreading, Issues and solutions

Unit 5:

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

Unit 6:

Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

References:

- Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition
- Kai Hwang, “Advanced Computer Architecture”, TMH
- V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.
- William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition
- Kai Hwang, Zhiwei Xu, “Scalable Parallel Computing”, MGH
- David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.

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MTVD15 (B).SYSTEM DESIGN WITH EMBEDDED

Unit 1:

Embedded Linux Vs Desktop Linux, Embedded Linux Distributions

Unit 2:

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

Unit 3:

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules

Unit 4:

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

Unit 5

:Building and Debugging: Kernel, Root file system Embedded Graphics

Unit 6:

Case study of uClinux

References:

- Karim Yaghmour, “Building Embededd Linux Systems”, O'Reilly & Associates
- P Raghvan, Amol Lad, SriramNeelakandan, “Embedded Linux System Design and Development”, Auerbach Publications
- Christopher Hallinan, “Embedded Linux Primer: A Practical Real World Approach”, Prentice Hall, 2nd Edition, 2010.
- Derek Molloy, “Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014.

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MTVD15(C). VLSI DESIGN

Unit1

Introduction: Basic concept of integrated circuits and manufacturing, Design fundamental for digital CMOS circuits, Design Abstraction and circuit Validation.

Unit 2

CMOS circuit and Logic Design: CMOS Logic gate design, Basic Physical design, CMOS Logic structure, I /O Structure, Power and Delay consideration.

Unit 3

System Design: CMOS Chip Design, standard cells, Programmable gate array, Design Capture, Simulation and Verification.

Unit 4

Subsystem Design: Data Operation, CMOS Sub System Design, Memory and Control Strategies, PLA and ROM Implementation.

Unit 5

CAD system and Algorithms: CAD systems, Layout Analysis, Placement and Routing Algorithms, Timing Analysis, Optimization, Logic Synthesis and Simulation, Testability Issues.

Reference Books:

- Principal Of Cmos Design: A System Prospective By Waste And Eshraghin
- Vlsi Design: System On Silicon, Pearson Education
- Vlsi Technology By Sze S.M.Tmh
- Basic Vlsi Design, System And Circuits By Pucknil D.A. Phi
- Vhdl Primer By Bhaskar Star Galax Pub

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

AUDIT COURSE-I

1 ENGLISH FOR RESEARCH PAPER WRITING

UNIT I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT III

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT IV

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

UNIT V

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

2. DISASTER MANAGEMENT

UNIT I

Introduction

Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.U**Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem.Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And ConflictsNIT II

UNIT II

Disaster Prone Areas In India

Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics

UNIT III

Disaster Preparedness And Management

Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

UNIT IV

Risk Assessment

Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People’s Participation In Risk Assessment. Strategies for Survival.

UNIT V

Disaster Mitigation

Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.

SUGGESTED READINGS:

1. R. Nishith, Singh AK, “Disaster Management in India: Perspectives, issues and strategies “’New Royal book Company.
2. Sahni, Pardeep Et.Al. (Eds.),” Disaster Mitigation Experiences And Reflections”, Prentice Hall Of India, New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies” ,Deep &Deep Publication Pvt. Ltd., New Delhi.

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3. SANSKRIT FOR TECHNICAL KNOWLEDGE

UNIT I

- Alphabets in Sanskrit,
- Past/Present/Future Tense,
- Simple Sentences

UNIT II

- Order
- Introduction of roots
- Technical information about Sanskrit Literature

UNIT III

- Technical concepts of Engineering-Electrical, Mechanical,
- Architecture, Mathematics

Suggested reading

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD 21 ANALOG AND DIGITAL CMOS VLSI DESIGN

Unit 1:

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models.

Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

Unit 2:

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Unit 3:

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Unit 4:

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Commongate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Unit 5:

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

Unit 6:

Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

References:

- J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design
- perspective”, Prentice Hall electronics and VLSI series, 2nd Edition.
- Baker, Li, Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.
- BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
- Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford, 3rd
- Edition.
- R J Baker, “CMOS circuit Design, Layout and Simulation”, IEEE Inc., 2008.
- Kang, S. and Leblebici, Y., “CMOS Digital Integrated Circuits, Analysis and Design”,
- TMH, 3rdEdition.
- Pucknell, D.A. and Eshraghian, K., “Basic VLSI Design”, PHI, 3rd Edition.

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MTVD 22 VLSI DESIGN VERIFICATION AND TESTING

Unit 1:

Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

Unit 2:

Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typed Of , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

Unit 3:

Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Unit 4:

SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying

objects, Public vs. Local, Straying off course building a testbench.

Unit 5:

Randomization: Introduction, What to randomize, Randomization in SystemVerilog,

Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints,

In-line constraints, The pre_randomize and post_randomize functions,

Unit 6:

Random number functions, Constraints tips and techniques, Common randomization

problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.

References:

- Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
- M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware
- Design,Specification, and Verification Language). System Verilog website – www.systemverilog.org
- http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
- General reuse information and resources www.design-reuse.com
- OVM, UVM(on top of SV) www.verificationacademy.com
- Verification IP resources
- http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
- http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD23 (A) .MEMORY TECHNOLOGIES

Unit 1:

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Unit 2:

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

Unit 3:

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs,Floating GateEPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit 4:

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation HardeningTechniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit 5 :

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Unit 6:

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues,
Memory Cards, High Density Memory Packaging

References:

- Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
- Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
- Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

MTVD23(B).SoC DESIGN

Unit 1:

ASIC

- Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit 2:

NISC

- NISC Control Words methodology, NISC Applications and Advantages, ArchitectureDescription Languages (ADL) for design and verification of Application Specific Instructionset Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Unit 3:

Simulation

- Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Unit 4:

Low power SoC design / Digital system,

- Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5 :

Synthesis

- Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trailspaths, connectivity, components, mapping/visualization, nodal and admittance graph.Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysisSingle core and Multi core systems, dark silicon issues,HDL coding techniques for minimization of power consumption, Fault tolerant designs

Unit 6:

Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

Note: Students will prepare and present a term paper on relevant identified current topics (inbatches of three students per topic) as a part of theory course.

References:

- Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
- B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
- RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center,2000
- P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
- Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley 2011

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD23(C) LOW POWER VLSI DESIGN

Unit 1:

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree Of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network.

Unit 4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers.

Unit 5: Low Power Memory Design: Sources & reduction of power dissipation in memorysubsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Unit 6: Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

References:

- P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer
- Academic, 2002
- Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.
- J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
- A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
- Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD 24(A).Communication Buses and Interfaces

Unit 1:

Serial Busses

- Physical interface, Data and Control signals, features,

Unit 2:

limitations and applications of RS232, RS485, I2C, SPI

Unit 3:

CAN - Architecture, Data transmission, Layers, Frame formats, applications

Unit 4:

PCIe - Revisions, Configuration space, Hardware protocols, applications

Unit 5:

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

Unit 6:

Data Streaming Serial Communication Protocol

- Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

References:

- Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for
- Embedded Systems ”, Lakeview Research, 2nd Edition
- Jan Axelson, “USB Complete”, Penram Publications
- Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
- Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media
- Corporation, 2nd Edition, 2005.
- Serial Front Panel Draft Standard VITA 17.1 – 200x
- Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

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MTVD24(B).NETWORK SECURITY AND CRYPTOGRPHY

Unit 1:

Security

- Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Unit 2:

Number Theory

- Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit 3:

Private-Key (Symmetric) Cryptography

- Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit 4:

Public-Key (Asymmetric) Cryptography

- RSA, Key Distribution and Management,Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Unit 5:A

Uthentication

- IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Unit 6:

System Security

- Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

References:

- William Stallings, “Cryptography and Network Security, Principles and Practices”,
- Pearson Education, 3rd Edition.
- Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private
- Communication in a Public World”, Prentice Hall, 2nd Edition
- Christopher M. King, ErtemOsmanoglu, Curtis Dalton, “Security Architecture, Design
- Deployment and Operations”, RSA Pres,
- Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey,
- “Inside Network Perimeter Security”, Pearson Education, 2nd Edition
- Richard Bejtlich, “The Practice of Network Security Monitoring: Understanding Incident Detection and Response”, William Pollock Publisher, 2013.

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MTVD24(C) PHYSICAL DESIGN AUTOMATION

Unit 1:

Introduction to VLSI Physical Design Automation.

Unit 2:

Standard cell, Performance issues in circuit layout, delay models Layout styles.

Unit 3:

Discrete methods in global placement.

Unit 4:

Timing-driven placement. Global Routing Via Minimization.

Unit 5:

Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.

Unit 6:

Compaction, algorithms, Physical Design Automation of FPGAs..

References:

- William Stallings, “Cryptography and Network Security, Principles and Practices”, Pearson Education, 3rd Edition.
- Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private
- Communication in a Public World”, Prentice Hall, 2nd Edition
- Christopher M. King, ErtemOsmanoglu, Curtis Dalton, “Security Architecture, Design Deployment and Operations”, RSA Pres,
- Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, “Inside Network Perimeter Security”, Pearson Education, 2nd Edition
- Richard Bejtlich, “The Practice of Network Security Monitoring: Understanding Incident Detection and Response”, William Pollock Publisher, 2013.

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AUDIT COURSE-II

1. CONSTITUTION OF INDIA

UNIT I

Introduction and Methodology:

- Aims and rationale, Policy background, Conceptual framework and terminology
- Theories of learning, Curriculum, Teacher education.
- Conceptual framework, Research questions**.**
- Overview of methodology and Searching.

UNIT II

. Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries.

- Curriculum, Teacher education

UNIT III

. Evidence on the effectiveness of pedagogical practices

- Methodology for the in depth stage: quality assessment of included studies.
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?
- Theory of change.
- Strength and nature of the body of evidence for effective pedagogical practices.
- Pedagogic theory and pedagogical approaches.
- Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV

. Professional development: alignment with classroom practices and follow-up support

- Peer support
- Support from the head teacher and the community.
- Curriculum and assessment
- Barriers to learning: limited resources and large class sizes

UNIT V

Research gaps and future directions

- Research design
- Contexts

- Pedagogy
- Teacher education
- Curriculum and assessment
- Dissemination and research impact.

Suggested reading

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, ‘learning to read’ campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

2. STRESS MANAGEMENT BY YOGA

UNIT I

Definitions of Eight parts of yog. (Ashtanga)

UNIT II

Yam and Niyam.
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT III

Asan and Pranayam
i) Various yog poses and their benefits for mind & body
ii)Regularization of breathing techniques and its effects-Types of pranayam

Suggested reading

1. 'Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD31(A).COMMUNICATION NETWORK

Unit 1:

Introduction:

- Network Architecture, Performance

Unit 2:

Connecting nodes:

- Connecting links, Encoding, framing, Reliable transmission, Ethernet and Multiple access networks, Wireless networks

Unit 3:

Queuing models

- For a) one or more servers b) with infinite and finite queue size c) Infinite population Internetworking:

- Switching and bridging, IPv4, Addressing, Routing Protocols, Scale issues, Routers - Architecture, IPv6

Unit 4:

End-to-End Protocols: - Services, Multiplexing, De-multiplexing, UDP, TCP, RPC, RTP

Unit 5:

Congestion control and Resource Allocation - Issues, Queuing disciplines, TCP congestion control, Congestion Avoidance, QoS Applications: - Domain Name Resolution, File Transfer, Electronic Mail, WWW, Multimedia Applications

Unit 6:

Network monitoring – Packet sniffing tools such as Wireshark Simulations using NS2/OPNET

References:

- Larry L. Peterson, Bruce S, Devie, “Computer Networks” , MK, 5th Edition
- Aaron Kershenbaum, “Telecommunication Network Design Algorithms”, MGH,
- International Edition 1993.
- Vijay Ahuja, “Communications Network Design and Analysis of Computer
- Communication Networks”, MGH, International Editions.
- Douglas E. Comer, “Internetworking with TCP/IP”, Pearson Education, 6th Edition

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD31(B).SELECTED TOPICS IN MATHEMATICAL

Unit 1:

Probability and Statistics:

- Definitions, conditional probability, Bayes Theorem and independence.
- Random Variables: Discrete, continuous and mixed random variables, probability mass, probability

density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

Unit 2:

Special Distributions:

Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions.

- Pseudo random sequence generation with given distribution, Functions of a Random Variable

Unit 3:

Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.

- Stochastic Processes: Definition and classification of stochastic processes, Poisson process
- Norms, Statistical methods for ranking data

Unit 4:

Multivariate Data Analysis

- Linear and non-linear models, Regression, Prediction and Estimation
- Design of Experiments – factorial method
- Response surface method

Unit 5:

Graphs and Trees:

- Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring

Unit 6:

Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set,theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning tree

References:

- Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rd Edition
- C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2nd Edition
- Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons, 2001.
- Douglas C. Montgomery, "Design and Analysis of Experiments", John Wiley and Sons, 2001.
- B. A. Ogunnaike, "Random Phenomena: Fundamentals of Probability and Statistics for Engineers", CRC Press, 2010.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD31(C).NANO MATERIAL AND TECHNOLOGY

Unit 1:

Nanomaterials in one and higher dimensions,

Unit 2:

Applications of one and higher dimension nano-materials.

Unit 3:

Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics.

Unit 4:

carbon nanotubes – synthesis and applications

Unit 5:

Interdisciplinary arena of nanotechnology.

References:

- Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards, 2ndedn, John Wiley and Sons, 2009.
- Nanocrystalline Materials by A I Gusev and A ARempel, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
- Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn, 2010.
- Carbon Nanotubes: Synthesis, Characterization and Applications by Kamal K. Kar, Research Publishing Services; 1stedn, 2011, ISBN-13: 978-9810863975.

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MTVD 32(A).Business Analytics

Unit1:

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of BusinessAnalytics Process and organisation, competitive advantages ofBusiness Analytics.Statistical Tools: Statistical Notation, Descriptive Statistical methods,Review of probability distribution and data modelling, sampling andestimation methods overview.

Unit 2:

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology

Unit 3:

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization. Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

Unit 4:

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making

Unit 5:

Recent Trends in : Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Reference:

- Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
- Business Analytics by James Evans, persons Education.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD32(B).OPERATIONS RESEARCH

Unit 1:

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Unit 2

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex
method - sensitivity analysis - parametric programming

Unit 3:

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit 4

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit 5

Competitive Models,Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

References:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

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MTVD32(C) Cost Management of Engineering Projects

UNIT–I:

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II:

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT – III:

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV:

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT – V:

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R.Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

References:

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

SARVEPALLI RADHAKRISHNAN UNIVERSITY, BHOPAL

MTVD DP (I) Dissertation (PHASE I)

Dissertation-I will have mid semester presentation and end semester presentation. Mid semester presentation will include identification of the problem based on the literature review on the topic referring to latest literature available. End semester presentation should be done along with the report on identification of topic for the work and the methodology adopted involving scientific research, collection and analysis of data, determining solutions and must bring out individuals contribution. Continuous assessment of Dissertation – I and Dissertation – II at Mid Sem and End Sem will be monitored by the departmental committee.

MTVD DP(II) Dissertation (PHASE II)

Dissertation – II will be extension of the to work on the topic identified in Dissertation – I.

Continuous assessment should be done of the work done by adopting the methodology decided involving numerical analysis/ conduct experiments, collection and analysis of data, etc.There will be presubmission seminar at the end of academic term. After the approval the student has to submit the detail report and external examiner is called for the viva-voce to assess along with guide.

Guidelines for Dissertation Phase – I and II at M. Tech.

- As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
- The dissertation may be carried out preferably in-house i.e. department's laboratories and centers OR in industry allotted through department's T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of

Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.

- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, a record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work